Graphic Era
Deemed to be
University
DEHRADUN

NAAC
GRADE A+
ACCREDITED

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Dehradun-248002 Uttarakhand
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# Department of Electronics and Communication Engineering

# Master of Technology

# VLSI Design and Systems

# Curriculum

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# University Vision

**We visualize Graphic Era (Deemed to be University) as an internationally recognized, enquiry driven, ethically engaged diverse community, whose members work collaboratively for positive transformation in the world, through leadership in teaching, research and social action.**

# University Mission

**The mission of the university is to promote learning in true spirit and offering knowledge and skills in order to succeed as professionals. The university aims to distinguish itself as a diverse, socially responsible learning community with a high-quality scholarship and academic rigor.**

# Department Vision

**The Department visualizes itself to become leading centre of learning in the field of Electronics & Communication Engineering with academic excellence in research to produce self-motivated, creative, and socially responsible engineers and specialists, ready to take up challenges of industrial development with ethics and societal commitment.**

# Department Mission

**M1: To provide high quality contemporary education in the field of Electronics & Communication Engineering and professional ethics to its learners.**

**M2: To provide creative learning environment for the students to equip them with strong foundation for continuing higher education.**

**M3: To pursue research and develop insight knowledge of current and emerging technologies in Electronics & Communication Engineering to serve the needs of the society, industry, and scientific community.**

**M4: To prepare students to have creative and innovative thinking to develop them into socially responsible professionals**

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# Program Educational Objectives (PEOs):

| | |
|---|---|
| **PEO1** | **Implementation of core-engineering knowledge to solve practical problems in the areas of VLSI design and Systems, and to produce innovative systems in these domains.** |
| **PEO2** | **Motivating entrepreneurship in VLSI domains by integration of sustainability with efficiently designed systems.** |
| **PEO3** | **Sharpening the educational, and research-oriented skills of the students for their easy merger into a future career in research or academia.** |
| **PEO4** | **Developing the design engineers with excellent ability to communicate, along with a morally responsible behavior.** |

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# Program Outcomes (POs):

| | |
|---|---|
| **PO1** | **Apply the knowledge of science, mathematics, and engineering principles for developing problem solving attitude.** |
| **PO2** | **Identify, formulate, and solve engineering problems in the broad areas like System Design using VLSI.** |
| **PO3** | **Use different modern engineering software tools in the domain of VLSI and Systems Design.** |
| **PO4** | **Design and conduct experiments, analyze and interpret data, imbibe programming skills for development of simulation experiments.** |
| **PO5** | **Function as a member of a multidisciplinary team with sense of ethics, integrity, and social responsibility.** |
| **PO6** | **Realize the need for self-education and ability for independent and life-long learning.** |

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# Program Specific outcomes (PSOs):

| | |
|---|---|
| **PSO1** | **Attain competency in areas of IC designing, testing, and developing prototype of various VLSI circuits.** |
| **PSO2** | **Integrating various VLSI sub-systems to design industrial circuits.** |
| **PSO3** | **Students gain skills in developing various complicated circuits and excel in industrial sector.** |

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# Program Course Structure (All Semesters)

## M. Tech (VLSI Design and Systems)
## (Batch 2022 onwards)
## Semester I

| Course Module | | | | | Teaching Periods | | | Weightage: Evaluation | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Theory Subjects | | | | | | | | | | | |
| Sl. No. | Code | Course title | Component | Credits | L | T | P | CWA | MSE | ESE | Total |
| 1 | VDM 101 | Semiconductor Materials and Devices | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 2 | VDM 102 | CMOS Analog Circuit Design | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 3 | VDM 103 | Advanced Digital Integrated Circuit | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 4 | VDM 104 | VLSI Technology | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 5 | VDM --- | Program Elective-I | PE | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| Laboratory and Others | | | | | | | | | | | |
| 6 | VDM 151 | CMOS Analog Circuit Design Lab | PC | 2 | 0 | 0 | 4 | 25 | 25 | 50 | 100 |
| 7 | VDM 152 | Digital VLSI Circuit Design Lab | PC | 2 | 0 | 0 | 4 | 25 | 25 | 50 | 100 |
| 8 | GP101 | General Proficiency | GP | 1 | 0 | 0 | 0 | 0 | 0 | 100 | 100 |
| | | **TOTAL** | | **20** | **15** | **00** | **08** | | | | **800** |

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# M. Tech (VLSI Design and Systems)
## (Batch 2022 onwards)
## Semester II

| Course Module | | | | | Teaching Periods | | | Weightage: Evaluation | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Theory Subjects** | | | | | | | | | | | |
| **Sl. No.** | **Code** | **Course title** | **Component** | **Credits** | **L** | **T** | **P** | **CWA** | **MSE** | **ESE** | **Total** |
| 1 | VDM 201 | Advanced ASIC and FPGA Design | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 2 | VDM 202 | Digital System Design using Verilog HDL | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 3 | VDM 203 | Advanced VLSI Circuit Testing | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 4 | VDM 204 | Low Power VLSI Design | PC | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 5 | VDM ____ | Program Elective-II | PE | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| **Laboratory and Others** | | | | | | | | | | | |
| 6 | VDM 251 | Verilog HDL Lab | PC | 2 | 0 | 0 | 4 | 25 | 25 | 50 | 100 |
| 7 | VDM 252 | VLSI Physical Design Lab | PC | 2 | 0 | 0 | 4 | 25 | 25 | 50 | 100 |
| 8 | VDM 253 | Mini Project with Seminar | PROJ | 2 | 0 | 0 | 4 | 25 | 0 | 75 | 100 |
| 9 | GP 201 | General Proficiency | GP | 1 | 0 | 0 | 0 | 0 | 0 | 100 | 100 |
| | | **TOTAL** | | **22** | **15** | **00** | **12** | | | | **900** |

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# M. Tech (VLSI Design and Systems)
## (Batch 2022 onwards)
## Semester III

| Course Module | | | | | Teaching Periods | | | Weightage: Evaluation | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Theory Subjects** | | | | | | | | | | | |
| **Sl. No.** | **Code** | **Course title** | **Component** | **Credits** | **L** | **T** | **P** | **CWA** | **MSE** | **ESE** | **Total** |
| 1 | VDM _____ | Program Elective-III | PE | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| 2 | VOM _____ | Open Elective | OE | 3 | 3 | 0 | 0 | 25 | 25 | 50 | 100 |
| **Laboratory and Others** | | | | | | | | | | | |
| 3 | VDM 351 | Modelling and Simulation Lab | PC | 2 | 0 | 0 | 4 | 25 | 25 | 50 | 100 |
| 4 | VDM 301 | Dissertation Phase-I* | PROJ | 10 | 0 | 0 | 20 | 25 | 50 | 125 | 200 |
| 5 | GP 301 | General Proficiency | GP | 1 | 0 | 0 | 0 | 0 | 0 | 100 | 100 |
| | | **TOTAL** | | **19** | **06** | **00** | **24** | | | | **600** |

***Students going for Industrial Project/Thesis will complete these courses through MOOCs.**

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# M. Tech (VLSI Design and Systems)
## (Batch 2022 onwards)
## Semester IV

| Course Module | | | | | Teaching Periods | | | Weightage: Evaluation | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Sl. No. | Code | Course title | Component | Credits | L | T | P | CWA | MSE | ESE | Total |
| 1 | VDM 401 | Dissertation Phase-II | PROJ | 16 | 0 | 0 | 32 | 50 | 100 | 250 | 400 |
| 2 | GP 401 | General Proficiency | GP | 1 | 0 | 0 | 0 | 0 | 0 | 100 | 100 |
| | | **TOTAL** | | **17** | **00** | **00** | **32** | | | | **500** |

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# M. Tech (VLSI Design and Systems)
## (Batch 2022 onwards)
## Program Electives and Open Electives

| Program Elective Courses | | |
|---|---|---|
| **Course Code** | **Course Name** | **Semester** |
| **Program Elective I** | | |
| VDM 191 | Advanced Nanotechnology | First |
| VDM 192 | Optimization Techniques in VLSI Design | |
| VDM 193 | Theory and Application of Embedded Systems | |
| VDM 194 | Digital Signal Processing for VLSI | |
| VDM 195 | Robust Control System | |
| VDM 196 | Control of Advanced Electric Machine | |
| **Program Elective II** | | |
| VDM 291 | Micro-Sensors and MEMS | Second |
| VDM 292 | RF Microelectronics Devices | |
| VDM 293 | VLSI Circuits for Biomedical Application | |
| VDM 294 | Microwave & MM-wave Integrated Circuits and Applications | |
| VDM 295 | Renewable Energy Resources and Energy Management | |
| VDM 296 | Multivariable Control System | |
| **Program Elective III** | | |
| VDM 391 | Organic Electronics Devices and Circuits | Third |
| VDM 392 | Memory Design and Testing | |
| VDM 393 | System on Chip Design and Testing | |
| VDM 394 | VLSI Physical Design Automation | |
| VDM 395 | Power Quality Assessment | |
| VDM 396 | Optimal & Adaptive Control | |

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## Open Elective Courses

| Course Code | Course Name | Semester |
|---|---|---|
| VOM 301 | Cloud Computing | Third |
| VOM 302 | Internet of Things | |
| VOM 303 | Artificial Intelligence and expert systems | |
| VOM 304 | Soft Computing | |

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# Abbreviations:

| | |
|---|---|
| L | Lecture |
| T | Tutorial |
| P | Practical |
| CWA | Class Work Assessment |
| MSE | Mid Semester Exam |
| ESE | End Semester Exam |
| PC | Program Core |
| PE | Program Elective |
| OE | Open Elective |
| PROJ | Project |
| GP | General Proficiency* |

*Institution Initiative

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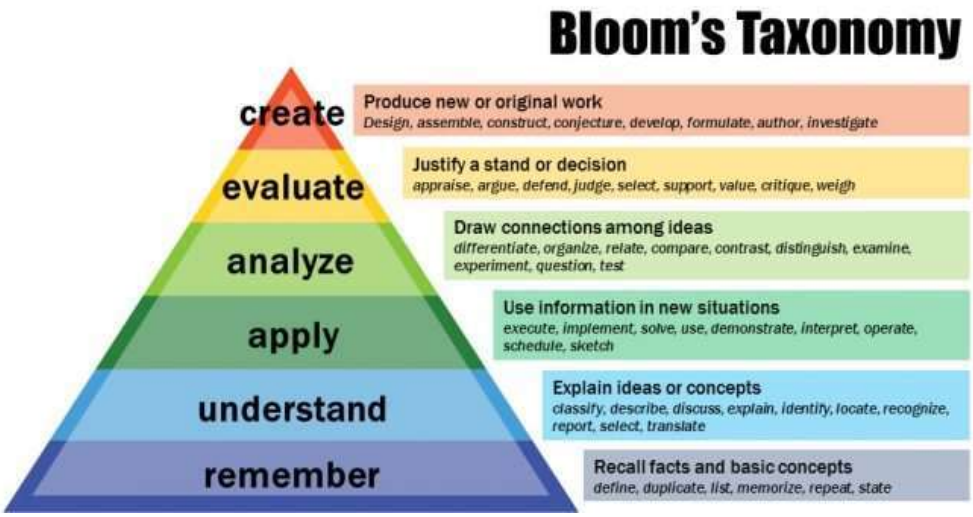
# Bloom's Taxonomy for Curriculum Design and Assessment

**Preamble**

**The design of curriculum and assessment is based on Bloom's Taxonomy. A comprehensive guideline for using Bloom's Taxonomy is given below for reference.**



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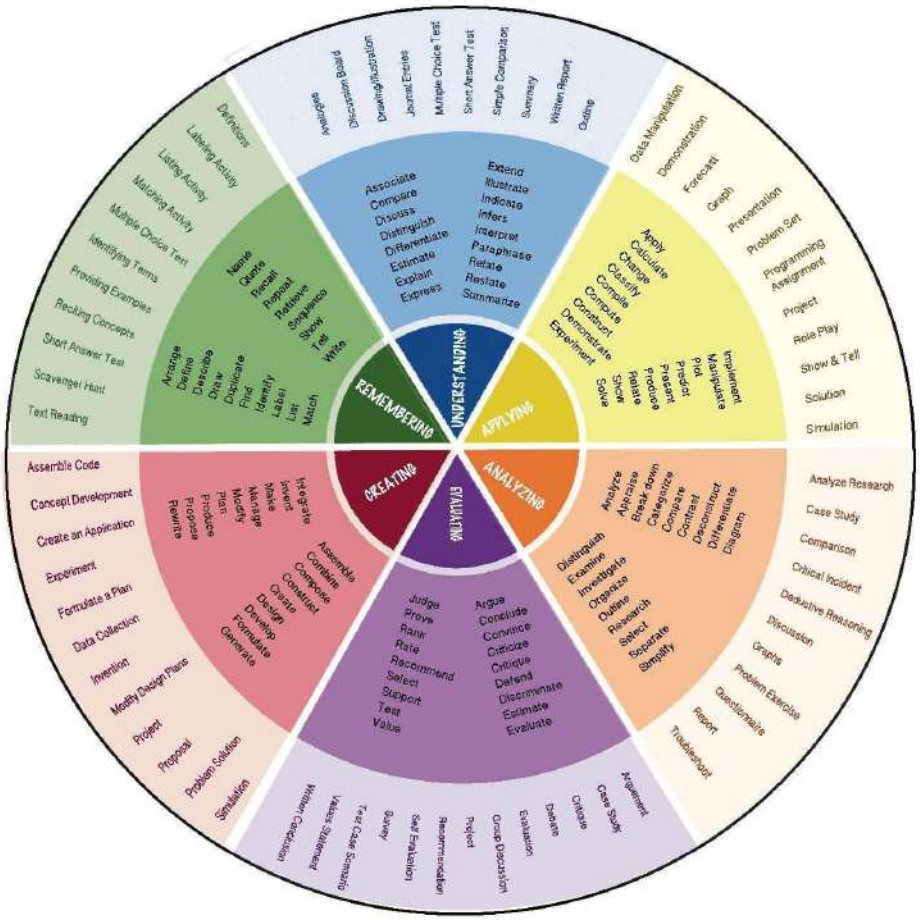

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Semiconductor Materials and Devices | | ***Code*** | VDM 101 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Electronics Engineering, Electronic Devices and Circuits | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Create** basic understanding of semiconductor device physics. |
| ***CO 2*** | **Evaluate** two terminal MOS structure in terms of its electrical parameters. |
| ***CO 3*** | **Analyse** the three terminal MOS structure in terms of electrical potential and charge. |
| ***CO 4*** | **Apply** surface potential and charges in different regions of MOSFET operation. |
| ***CO 5*** | **Understand** the short channel and narrow channel effects. |
| ***CO 6*** | **Implement** the concepts of semiconductor device physics in developing real life applications. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Basics of Semiconductors:** Semiconductor materials, Energy levels, Intrinsic and extrinsic semiconductor, Equilibrium in absence/presence of electric field. | 8 |
| ***Unit 2:*** | **PN Junction Diode:** Junction diode: PN junction, Tunnel diode, Quasi-fermi levels, Depletion width capacitance and its application in doping profile determination, I-V characteristics of narrow and wide base diodes and their equivalent circuits, Breakdown mechanisms, Small signal ac impedance. | 8 |
| ***Unit 3:*** | **Two Terminal MOS Structure:** Flat band voltage, Potential balance and charge balance, Effect of gate body voltage on surface condition, Accumulation, Depletion, Inversion, General analysis, Small signal capacitance. | 10 |
| ***Unit 4:*** | **Three Terminal MOS Structure:** Contacting the inversion layer, Body effect, Different regions of operation, Pinch-off voltage. | 10 |
| ***Unit 5:*** | **Four Terminal MOS Structure:** Transistors regions of operation, Complete all-region model, Simplified all-region model, Models based on quasi fermi potential, Regions of inversion in terms of terminal voltage, Temperature effects, Breakdown, Enhancement mode, Depletion mode transistors. | 6 |
| **Total Hours** | | **42** |

| ***Textbooks*** | |
|---|---|
| **1.** | Tsividis, Yannis, and Colin McAndrew, "***Operation and Modelling of the MOS Transistor***", Oxford: Oxford University Press, Vol. 2, 3rd Edition, 2003. |

## Semester I

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| | |
|---|---|
| **2.** | S. Kang and Y. Leblebici, "***CMOS Digital Integrated Circuits, Analysis and Design***", 3rd Edition, Tata McGraw-Hill, 2003. |
| | ***Reference Books*** |
| **3.** | Robert L. Boylestad and Louis Nashelsky, "***Electronic Devices and Circuit Theory***", 9th Edition, Prentice Hall of India (PHI), 2006. |
| **4.** | Ben g. Streetman and Sanjay Kumar Banerjee, "***Solid State Electronic Devices***", 6th Edition, Prentice Hall of India (PHI), 2013. |
| **5.** | Takayasu Sakurai, Akira Matsuwawa and Takakuni Douseki, "***Fully-Depleted SOI CMOS Circuits and Technology for Ultralow power applications***", 1st Edition, Springer, 2006. |


| | |
|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| *Master of Technology* | | | | | | |
| *VLSI Design and Systems* | | | | | | |
| ***Semester*** | First | ***Subject Title*** | CMOS Analog Circuit Design | | ***Code*** | VDM 102 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Electronics Devices and Circuits | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the knowledge of analog IC design in CMOS technologies. |
| ***CO 2*** | **Understand** MOS transistors with different configurations. |
| ***CO 3*** | **Apply** the concepts of multistage and differential MOS amplifiers. |
| ***CO 4*** | **Analyse** the current mirror circuits. |
| ***CO 5*** | **Assess** and evaluation the feedback amplifiers and phase locked loop. |
| ***CO 6*** | **Design** and **develop** various CMOS analog circuits. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Models for Integrated Circuit Active Devices:** The depletion region of a PN junction, Depletion region capacitance and junction breakdown, Basics of MOS transistor, Derivation of current-voltage relationship, Analysis of MOS as an amplifier, Small signal models of MOS transistor, MOS transistor frequency response. | 8 |
| ***Unit 2:*** | **Single Stage Amplifier:** Common source stage with resistive load, CS stage with diode connected load, CS stage with current source load, CS stage with triode load, CS stage with source generation, Source follower and common gate configuration. | 9 |
| ***Unit 3:*** | **Multistage Amplifier and Operational Amplifier:** Cascode current source, Cascode amplifier, Differential pair, Small and large signal analysis of differential amplifier, Differential amplifier with MOS loads, OPAMP design: General consideration, One stage OpAmp | 9 |
| ***Unit 4:*** | **Current Mirrors, Active Loads and References:** Simple current mirror, Cascode current mirror, Wilson current mirror, Common source amplifier with complementary load, Voltage and current references: Widlar and peaking current sources, supply insensitive biasing. | 9 |
| ***Unit 5:*** | **Feedback and Non-Linear Analog Circuits:** General consideration, Properties of feedback circuits, Feedback configuration, Nonlinear analog circuits: LC oscillators, Simple phase locked loop. | 9 |
| **Total Hours** | | **44** |

| ***Textbooks*** | |
|---|---|
| **1.** | B. Razavi, "***Design of analog CMOS Integrated Circuits***", McGraw-Hill, 1st Edition, 2002. |
| **2.** | Mohammed Ismail and Terri Faiz, "***Analog VLSI Signal and Information Process***", McGraw-Hill, 1st Edition, 1994. |

## Semester I

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| | |
|---|---|
| | ***Reference Books*** |
| **3.** | Paul R. Gray and R. G. Meyer, "***Analysis and Design of Analog Integrated Circuits***" John Wiley and Sons", 4th Edition, 2001. |
| **4.** | R. Jacob Baker, H. W. Li, and D.E. Boyce, "***CMOS: Circuit Design, Layout and Simulation***", Prentice-Hall of India, 3rd Edition, 2010. |

| | |
|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| *Master of Technology* | | | | | | |
| *VLSI Design and Systems* | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Advanced Digital Integrated Circuit | | ***Code*** | VDM 103 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:***Basic Electronics Engineering and Digital Electronics | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Describe** the basic MOS structure and layout design. |
| ***CO 2*** | **Understand** the static and dynamic characteristics of MOS inverters. |
| ***CO 3*** | **Apply** the MOS concepts to design combinational and sequential MOS logic circuits. |
| ***CO 4*** | **Analyse** different digital MOS logic circuits. |
| ***CO 5*** | **Estimate** power consumption of CMOS logic circuits. |
| ***CO 6*** | **Integrate** various concepts of digital VLSI circuit design and apply them in **designing** of MOS based digital circuits. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction and Implementation of strategies for digital ICs:** Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design, Design rule: Stick diagram and layout. Custom Circuit design, Cell based and Array based design implementations. | 10 |
| ***Unit 2:*** | **MOS Inverters:** Static and Dynamic Characteristics of CMOs inverter, Power dissipation, Logical effort. | 10 |
| ***Unit 3:*** | **Designing combinational and sequential circuits:** Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and dynamic properties of complex gates, Dynamic CMOS Logic. Timing metrics of sequential circuits, Dynamic latches and Registers. Pipelining. | 10 |
| ***Unit 4:*** | **Interconnect and Timing Issues:** Circuit characterization and performance estimation - Resistance, Capacitance estimation - Switching characteristics - Delay models –Timing issues in Digital circuits, Power dissipation. Impact of Clock Skew and Jitter. | 6 |
| ***Unit 5:*** | **Memory Design:** Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers | 6 |
| **Total Hours** | | **42** |

| ***Textbooks*** | |
|---|---|
| **1.** | S. Kang and Y. Leblebici, "***CMOS Digital Integrated Circuits, Analysis and Design***", Tata McGraw-Hill, 3rd Edition, 2003. |

## Semester I

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| | |
|---|---|
| **2.** | J. M. Rabaey, A. Chandrakasan and B. Nikolic, "***Digital Integrated Circuits: A Design Perspective***", Prentice-Hall of India, 2nd Edition, 2006. |
| | ***Reference Books*** |
| **3.** | John P. Uyemura, "***Introduction to VLSI Circuits***", Wiley India Pvt. Ltd,1st Edition 2012 |
| **4.** | Eugene Fabricius, "***Introduction to VLSI Design"***, New Ed Edition, Tata McGraw - Hill Education, 1990 |
| **5.** | N. H. E. Weste et. al., "***CMOS VLSI Design***", Pearson, 3rd Edition, 2005. |
| **6.** | R. Jacob Baker, "***CMOS: circuit design, layout, and simulation***", John Wiley & Sons, 3rd Edition, 2010. |


| | |
|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | VLSI Technology | | ***Code*** | VDM 104 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** VLSI Technology and Design | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Explain** about wafer fabrication techniques and oxidation process. |
| ***CO 2*** | **Analyse** photolithography and etching techniques of VLSI design. |
| ***CO 3*** | **Extend** the knowledge of different physical and chemical deposition methods. |
| ***CO 4*** | **Investigate** metal deposition techniques and IC fabrication methodologies. |
| ***CO 5*** | **Design** and **analysis** of different packaging methods. |
| ***CO 6*** | **Create** a base for the semiconductor device fabrication using VLSI technology. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Wafer Preparation and Oxidation:** Electron grade silicon, Crystal growth, Wafer preparation, Processing considerations, Vapor phase epitaxy and molecular beam epitaxy, Film characteristics, SOI structure, Oxide formation, Kinetics, Oxidation systems, Dry and wet oxidation, Masks properties of $SiO_2$, Oxidation defects, Redistribution of dopant at interface, Oxidation of poly silicon. | 10 |
| ***Unit 2:*** | **Lithography and Etching:** Optical, Electron, X-Ray and Ion Lithography methods, Positive and negative photo resist. Plasma properties, Size, Control, Etch mechanism, Etch techniques and equipment. | 8 |
| ***Unit 3:*** | **Deposition and diffusion:** Deposition process and methods, Diffusion in solids, Diffusion equation and Diffusion mechanisms, Flick's one-dimensional diffusion equation, Atomic diffusion mechanism, Measurement techniques, Range theory, Implant equipment, Ion implantation, Damage and annealing, Ion implantation systems. | 8 |
| ***Unit 4:*** | **Metallization and IC Fabrication:** Metallization and its applications, Process simulation of Ion implementation, Diffusion, Oxidation, Epitaxy, Lithography, Etching and deposition, Annealing shallow junction – High energy implantation, Physical vapours deposition patterning. NMOS, CMOS and bipolar IC technologies and IC fabrication. | 8 |
| ***Unit 5:*** | **Fin-FET Process Flow and Packaging:** Fin-FET manufacturing technology, Bulk Fin-FET fabrication, SOI Fin-FET process flow. Analytical and assembly techniques and packaging of VLSI devices. | 8 |
| **Total Hours** | | **42** |

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| | |
|---|---|
| | ***Textbooks*** |
| **1.** | S. M. Sze, "***VLSI Technology***", McGraw Hill, 2nd Edition, 1988. |
| **2.** | W. Wolf, "***Modern VLSI Design***", Pearson, 3rd Edition, 2002. |
| | ***Reference Books*** |
| **3.** | S. K. Gandhi, "***VLSI Fabrication Principles Silicon and Gallium Arsenide***", Wiley-INDIA, 2nd Edition, 1994. |
| **4.** | Wai Kai Chen, "***VLSI Technology***", CRC press, 1st Edition, 2003. |
| **5.** | Samar K Saha,, "***FinFET Devices for VLSI Circuits and Systems",*** CRC Press, 1st Edition, 2020. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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**Semester I**

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | CMOS Analog Circuit Design Lab | | ***Code*** | VDM 151 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 02 | | 0 | 0 | 4 |
| ***Examination Duration (Hrs)*** | | ***Practical*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Electronics Devices and Circuit, VLSI Technology and Design | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Understand** Cadence Virtuoso simulation tool. |
| ***CO 2*** | **Design** common source, common drain, and operational amplifier using Cadence tool. |
| ***CO 3*** | **Simulate** and **analyse** various CMOS based circuits using Cadence tool. |
| ***CO 4*** | **Integrate** the acquired knowledge for developing CMOS based circuits. |
| | |
| ***Exp. No.*** | ***Name of the Experiment*** |
| ***1.*** | Design a new cell view and build common source amplifier and create a symbol for the common source amplifier using 45 nm technology. |
| ***2.*** | Simulation of common source amplifier test circuit using common source amplifier symbol using 45 nm technology. |
| ***3.*** | Create a layout of common source amplifier using 45 nm technology. |
| ***4.*** | Design a new cell view and build common drain amplifier and create a symbol for the common drain amplifier using 45 nm technology. |
| ***5.*** | Simulation of common drain amplifier test circuit using common drain amplifier symbol using 45 nm technology. |
| ***6.*** | Create a layout of common drain amplifier using 45 nm technology. |
| ***7.*** | Design a new cell view and build Differential amplifier and create a symbol for the Differential amplifier using 45 nm technology. |
| ***8.*** | Simulation of Differential amplifier test circuit using Differential amplifier symbol using 45 nm technology. |
| ***9.*** | Create a layout of Differential amplifier using 45 nm technology. |
| ***10.*** | Design a new cell view and build operational amplifier and create a symbol for the operational amplifier using 45 nm technology. |
| ***11.*** | Simulation of operational amplifier test circuit using operational amplifier symbol using 45 nm technology. |
| ***12.*** | Create a layout of operational Amplifier using 45 nm technology. |
| **Innovative** | |
| ***13.*** | Design and simulation of current mirror circuits using 45 nm technology. |
| ***14.*** | Design and Simulation of Cascode amplifier using 45 nm technology. |
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Digital VLSI Circuit Design Lab | | ***Code*** | VDM 152 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 02 | | 0 | 0 | 4 |
| ***Examination Duration (Hrs)*** | | ***Practical*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Digital Electronics | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Understand** the CMOS based digital integrated circuits. |
| ***CO 2*** | **Analyse** CMOS based combinational circuits using 180 nm Technology. |
| ***CO 3*** | **Evaluate** CMOS based sequential circuits and memory devices. |
| ***CO 4*** | **Design** and **validate** various CMOS based digital circuits using Cadence tool. |

| ***Exp. No.*** | ***Name of the Experiment*** |
|---|---|
| ***1.*** | Design and comparison of DC and transient output characteristics of CMOS inverter at different aspect ratio. |
| ***2.*** | Draw a layout of CMOS inverter using 45 nm technology and check for LVS and DRC for inverter circuit. |
| ***3.*** | Design and implement various gates with CMOS logic along with its layout. |
| ***4.*** | Draw a schematic of half adder/full adder using 45 nm technology and analyse its transient characteristics. |
| ***5.*** | Draw the layouts of half adder/full adder using 45 nm technology and simulate its transient characteristics. |
| ***6.*** | Design a schematic of comparator using 45 nm technology and simulate its transient characteristics |
| ***7.*** | Design and Implementation of 2:1 Multiplexer and 1:2 Demultiplexer. |
| ***8.*** | Design the schematic of latches using 45 nm technology and simulate its transient characteristics |
| ***9.*** | Design the schematic of flip-flops using 45 nm technology and simulate its transient characteristics |
| ***10.*** | Design the schematic of shift register using 45 nm technology and simulate its transient characteristics |
| ***11.*** | Design the schematic of up/down counter using 45 nm technology and simulate its transient characteristics |
| ***12.*** | Design the schematic of 6T RAM using 45 nm technology and simulate its transient characteristics |
| **Innovative** | |
| ***13.*** | Design and implementation of Flash Memory with Cadence tool. |
| ***14.*** | Design and implementation of Different Analog to Digital converter (ADC) with Cadence tool. |
| ***15.*** | Simulate substrate bias (Body) effect in CMOS inverter. |

| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam |
|---|---|

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|---|---|---|---|---|---|---|
| ***Course:- Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Advanced ASIC and FPGA Design | | ***Code*** | VDM 201 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Advanced Digital Integrated Circuit | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| ***CO 1*** | **Describe** the concepts of ASICs, CMOS Logic and ASIC Library Design. |
| ***CO 2*** | **Understanding** about partitioning, floor planning, placement and routing including circuit extraction of ASIC |
| ***CO 3*** | **Applying** the concepts of ASIC and FPGA in designing various architecture of different types of FPGA. |
| ***CO 4*** | **Analysis** of the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design. |
| ***CO 5*** | **Evaluation** of SOC based integrated circuits for various FPGA applications |
| ***CO 6*** | **Designing** of ASIC family using Xilinx tool to optimize the device performance. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction**:<br>Types of ASICs, Design flow, CMOS transistors CMOS design rules, Combinational logic cell, Sequential logic cell, Transistors as resistors, Transistor parasitic capacitance, Logical effort, Library cell design, Library architecture. | 10 |
| ***Unit 2:*** | **ASIC Physical Design**<br>System partition, partitioning, partitioning methods, interconnect delay models and measurement of delay, floor planning, placement, Routing, Circuit extraction, DRC. | 9 |
| ***Unit 3:*** | **FPGA Architecture:**<br>Field Programmable gate arrays, Logic blocks, routing architecture, Design flow technology, Xilinx XC4000, ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance Case studies: Altera MAX 5000 and 7000, Altera MAX 9000, Spartan II and Virtex II FPGAs | 10 |
| ***Unit 4:*** | **Trade off issues at System Level**<br>Optimization with regard to speed, area and power, asynchronous and low power system design. ASIC physical design issues, System Partitioning, Power Dissipation, Partitioning Methods | 8 |
| ***Unit 5:*** | **System On Chip Design**<br>Design using Xilinx Family, System on Chip Design, SoC Design Flow, Platform based and IP based SoC designs, Basic Concept of Bus – Based | 8 |

## Semester II

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| | | |
|---|---|---|
| | communication architectures, On- chip communication architectures standards, Low power SoC designs | |
| **Total Hours** | | **45** |

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|---|---|
| | ***Textbooks*** |
| **1.** | M.J.S .Smith, "***Application - Specific Integrated Circuits***", Addison –Wesley Longman Inc., Pearson Education, 1st Edition, 2008. |
| **2.** | Pasricha and N.Dutt, "***On-Chip Communication Architectures System on Chip Interconnect",*** Elsveir", 1st Edition, 2008, . |
| | ***Reference Books*** |
| **3.** | M. Rabaey, A. Chandrakasan, and B.Nikolic, "***Digital Integrated Circuit Design Perspective*** ", 2nd Edition, PHI 2003. |
| **4.** | Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, **"Low-Power NoC for High-Performance SoC Design"**, CRC Press, 1st Edition, 2008. |
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Digital System Design using Verilog HDL | | ***Code*** | VDM 202 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Digital Electronics | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Describe** digital circuits and its implementation through Verilog HDL code. |
| ***CO 2*** | **Understand** the concept of logic synthesis using Verilog HDL, and its impact in verification |
| ***CO 3*** | **Design** various combinational and sequential circuits. |
| ***CO 4*** | **Analyse** user defined primitives in Verilog HDL. |
| ***CO 5*** | **Apply** the knowledge of different types of digital modelling in Verilog HDL. |
| ***CO 6*** | **Justify** the implementation of Verilog code of several digital circuits using Verilog HDL and their test benches. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Basic Concepts:**<br>Lexical conventions, Data types, System tasks and compiler directives.<br>**Modules and Ports:**<br>Modules, Ports, Hierarchical names.<br>**Gate-Level Modeling:**<br>Gate types, Gate delays. | 8 |
| ***Unit 2:*** | **Dataflow Modelling:**<br>Continuous assignments, Delays, Expressions, Operators and Operands. Operator types, Examples.<br>**Behavioural Modelling:**<br>Structured procedures, Procedural assignments, Timing controls, Conditional statements, Multiway branching, Loops, Sequential and parallel Blocks, Generate blocks, Examples. | 10 |
| ***Unit 3:*** | **Task and Functions:**<br>Differences between tasks and functions, Tasks, Functions.<br>**Useful Modelling Techniques:**<br>Procedural continuous assignments, Overriding parameters, Conditional compilation and execution, Time scales, Useful system tasks.<br>**Timing and Delays:**<br>Types of delay models, Path delay modelling, Timing checks, Delay back-annotation | 8 |
| ***Unit 4:*** | **Switch-Level Modelling:**<br>Switch-Modelling elements, examples.<br>**User-Defined Primitives:**<br>UDP basics, Combinational UDPs, Sequential UDPs, UDP table shorthand symbols, Guidelines for UDP design. | 8 |
| ***Unit 5:*** | **Writing Test Benches:** | 8 |

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|---|---|---|
| | Basic test benches, Test bench structure, Constrained random stimulus generation, Object-oriented programming and Assertion-based verification. | |
| **Total Hours** | | **42** |

| | |
|---|---|
| | ***Textbooks*** |
| **1.** | Samir Palnitkar, "***Verilog HDL***", Pearson Education,2nd Edition, 2003. |
| **2.** | Mark Zwolinski, "***Digital System Design with System Verilog",*** *Pearson Education*, 1st Edition, 2009. |
| | ***Reference Books*** |
| **3.** | J. Bhasker, "***Verilog HDL Synthesis-A practical Prime***", Star galaxy Press,1st Edition, 1998 |
| **4.** | J. Bhasker, "***Verilog HDL Primer", Pearson Education***", 3rd Edition, 2015 |
| **5.** | Peter J. Ashenden, "***Digital Design: An Embedded Systems Approach Using VERILOG***", Elsevier, 1st Edition, 2008. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Advanced VLSI Circuit Testing | | ***Code*** | VDM 203 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** VLSI Technology | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Recall** the knowledge of fault modeling and fault simulation. | | | | | |
| ***CO 2*** | **Understand** ATPG algorithm for combinational and sequential circuits | | | | | |
| ***CO 3*** | **Apply** the knowledge of high-level testability Measures, SCOAP controllability and observability. | | | | | |
| ***CO 4*** | **Analyse** different memory testing algorithms. | | | | | |
| ***CO 5*** | **Assess** and **evaluate** scan architecture. | | | | | |
| ***CO 6*** | **Design** testing algorithms for VLSI components. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction:**<br>Role of testing, Digital and analog VLSI testing, VLSI technology trends affecting testing.<br>**VLSI Testing Process and Test Equipment:**<br>Types of testing, Automatic test equipment, Multi-Site testing, Electrical parametric testing.<br>**Test Economics and Product Quality:**<br>Defining costs, Production benefit-cost analysis, Economics of testable design, The rule of ten, Yield, Test data analysis.<br>**Fault Modelling:**<br>Defects, Errors and Faults, Functional versus Structural testing, A glossary of fault models, Single stuck-at fault,<br>**Logic and Fault Simulation:**<br>Simulation for design verification, Simulation for test evaluation | 10 |
| ***Unit 2:*** | **Testability Measures:**<br>SCOAP controllability and observability, High-level testability measures.<br>**Combinational Circuit Test Generation:**<br>Algorithms and representations, Redundancy identification (RID), Testing as a global problem, Definitions, Test generation systems, Test compaction, Significant combinational ATPG algorithms and sequential circuit test generation. | 8 |
| ***Unit 3:*** | **Memory Test:**<br>Memory density and defect trends, Faults, Memory test levels, March test notation, Fault modelling, Memory testing. Analog and mixed signal test, Delay test and IDDQ test. | 8 |
| ***Unit 4:*** | **Fundamental Techniques for Logic Testing:**<br>DFT fundamentals, ATPQ fundamental, Scan architecture and technique. | 8 |

## Semester II

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| ***Unit 5:*** | **Embedded Core Test Fundamentals:**<br>Introduction to embedded core testing, Core, Core-based design, Reuse core deliverables, Core DFT issues, Development of reusable core, Scan testing the isolated core, Scan testing the non-core logic, User defined logic chip-level DFT concerns, Memory testing with BIST. | 8 |
| **Total Hours** | | **42** |

| | |
|---|---|
| | ***Textbooks*** |
| **1.** | Viswani D. Agarval Michael L. Bushnell, "***Essentials of electronic testing for digital memory & mixed signal VLSI circuit***", Kluwer Academic Publications, 1st Edition ,1999. |
| **2.** | Alfred L. Crouch, "***Design for test for digital IC's and embedded core systems***", PHI, 1st Edition.1999. |
| | ***Reference Books*** |
| **3.** | Parag. K. Lala, "***Digital circuit testing and testability***", Academic Press, 1st Edition, 1997. |
| **4.** | Ashok K. Sharma, "***Semiconductor memories technology, testing and reliability***", Prentice-Hall of India Private Limited, New Delhi, 1st Edition, 1997. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| *Master of Technology* | | | | | | |
| *VLSI Design and Systems* | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Low Power VLSI Design | | ***Code*** | VDM 204 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Advanced Digital Integrated Circuit | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Acquire** the fundamental knowledge of low power VLSI design, |
| ***CO 2*** | **Infer** about static and dynamic power dissipation. |
| ***CO 3*** | **Ability** to implement logic circuits and advanced low power design techniques. |
| ***CO 4*** | **Analyse** different techniques required to minimize the leakage power. |
| ***CO 5*** | **Evaluate** the characteristics low power analog and digital circuits. |
| ***CO 6*** | **Design** of low power memory devices. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction to Low Power VLSI:** Overview, Need for Low Power VLSI Digital Integrated Circuits, Basic Principles of Low Power Design, Physics of Power Dissipation; Technology and Device Effect on Low Power**:** Transistor Sizing, Gate Oxide Thickness, Impact of Technology Scaling, Technology & Device innovation. | 10 |
| ***Unit 2:*** | **Sources of Power Dissipation in MOS Devices:** Power Estimation, Dynamic Power Dissipation: Short Circuit Power, Switching Power, Gliching Power; Static Power Dissipation, Probabilistic Power Analysis, Degrees of Freedom. | 8 |
| ***Unit 3:*** | **Logic Circuits and Advanced Techniques:** Logic circuits, Special Techniques: Architecture and Systems; Emerging Low power Techniques, Physics of Power Dissipation in CMOS FET Devices; Design of Low Power CMOS Circuits, Supply Voltage Scaling Approaches; Switched Capacitance minimization Approaches. | 8 |
| ***Unit 4:*** | **Leakage Power Minimization Approaches:** Synthesis in Low Power Design, Test of Low Voltages CMOS Circuits; Variable threshold Voltage CMOS (VTCMOS) Approach, Multi threshold Voltage CMOS (MTCMOS) approach, Power gating Transistor Stacking, Dual- threshold Voltage (Vt) Assignment Approach (DTCMOS). | 8 |
| ***Unit 5:*** | **Low Power Techniques:** Low Power Static RAM Architectures, Low Power SRAM/DRAM Design, Low Energy Computing using Energy Recovery Techniques, Software Design for Low Power, CAD Tools for Low Power Synthesis. | 8 |
| **Total Hours** | | **42** |

| ***Textbooks/ Reference Books:*** | |
|---|---|
| **1.** | Gary Yeap, "***Practical Low Power Digital VLSI Design***", Springer, 1st Edition, 1998. |

## Semester II

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|---|---|
| **2.** | Kaushik Roy and Sharat Prasad, "***Low Power CMOS VLSI Circuit Design***",1st Edition, 2000. |
| **3.** | J. B. Kuo and J. H. Lou, Low "***Voltage CMOS VLSI Circuits***", Wiley, 1st Edition, 1999. |
| **4.** | J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, "***Digital Integrated Circuits: A Design Perspective***", 2nd edition, Pearson, 2003. |


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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Verilog HDL Lab | | ***Code*** | VDM 251 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 02 | | 0 | 0 | 4 |
| ***Examination Duration (Hrs)*** | | ***Practical*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Digital Electronics | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Understand** digital circuit designing through Verilog HDL. | | | | | |
| ***CO 2*** | **Implement** digital logic circuits using Verilog HDL in FPGA. | | | | | |
| ***CO 3*** | **Analyse** various combinational and sequential circuits using Verilog HDL simulation codes. | | | | | |
| ***CO 4*** | **Design** various digital systems using Verilog HDL simulation codes. | | | | | |
| | | | | | | |
| ***Exp. No.*** | ***Name of the Experiment*** | | | | | |
| ***1.*** | Design and simulation of XOR gate using NAND gate only. | | | | | |
| ***2.*** | Design and simulation of comparator. | | | | | |
| ***3.*** | Design and simulation of Full Adder and Full Subtractor. | | | | | |
| ***4.*** | Design and simulation of Multiplexer and Demultiplexer. | | | | | |
| ***5.*** | Design and simulation of Encoder and Decoder. | | | | | |
| ***6.*** | Design and simulation of SR Flip-Flops and D Flip-flop. | | | | | |
| ***7.*** | Design and simulation of JK Flip-Flops and T Flip-flop. | | | | | |
| ***8.*** | Design and simulation of UP-DOWN counter/Decade counter. | | | | | |
| ***9.*** | Design and simulation of different registers. | | | | | |
| ***10.*** | Design and simulation of bidirectional and universal shift register | | | | | |
| ***11.*** | Design and simulation of binary multiplier. | | | | | |
| ***12.*** | FPGA Implementation of basics logic gates. | | | | | |
| ***13.*** | Design and simulation of Finite State Machine (FSM) using "Function" in Verilog. | | | | | |
| ***14.*** | Design and simulation of Finite State Machine (FSM) without using "Function" in Verilog. | | | | | |
| **Innovative** | | | | | | |
| ***15.*** | FPGA Implementation of Flip-flops. | | | | | |
| ***16.*** | FPGA Implementation of binary multiplier. | | | | | |
| ***17.*** | Design and simulation of floating-point divider. | | | | | |
| ***18.*** | As suggested by faculty and lab in-charge. | | | | | |

| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam |
|---|---|

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | VLSI Physical Design Lab | | ***Code*** | VDM 252 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 02 | | 0 | 0 | 4 |
| ***Examination Duration (Hrs)*** | | ***Practical*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Digital Electronics, Digital VLSI Circuit Design | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Understand** Linux environment, tools, and basic scripting. |
| ***CO 2*** | **Apply** the concepts of physical design for VLSI chip. |
| ***CO 3*** | **Analyse** placement, routing, and power Planning for different circuits. |
| ***CO 4*** | **Design** circuits using Verilog HDL, waveform Debugging, and synthesis. |

| ***Exp. No.*** | ***Name of the Experiment*** |
|---|---|
| ***1.*** | Familiarization with Linux environment, and basic scripting using Verilog HDL. |
| ***2.*** | Design, simulation, and test of an 8-bit counter with instructions using Verilog HDL. |
| ***3.*** | Synthesis of 8-bit counter circuit with instructions using Verilog HDL. |
| ***4.*** | Placement and power planning of 8-bit counter circuit in cadence digital implementation tool of 8-bit counter circuit. |
| ***5.*** | Routing of 8-bit counter circuit in cadence digital implementation tool in gpdk 90 technology. |
| ***6.*** | Design, simulation, and test of a Half adder with instructions using Verilog HDL. |
| ***7.*** | Synthesis of Half adder circuit with instructions using Verilog HDL. |
| ***8.*** | Placement and power planning of Half adder circuit in Cadence digital implementation tool of Half adder circuit. |
| ***9.*** | Routing of Half adder circuit in Cadence digital implementation tool in gpdk 90 technology. |
| ***10.*** | Design, simulation, and test of a Full adder with instructions using Verilog HDL. |
| ***11.*** | Design, simulation, and test of a Half subtractor with instructions using Verilog HDL. |
| ***12.*** | Synthesis of Half subtractor circuit with instructions using Verilog HDL. |
| **Innovative** | |
| ***13.*** | Design, simulation, and test of a Full subtractor with instructions using Verilog HDL. |
| ***14.*** | Routing of Full subtractor Circuit in Cadence Digital Implementation tool in gpdk 90 technology. |
| ***15.*** | Design, simulation, and Test of a Full subtractor with instructions using Verilog HDL. |

| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam |
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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | Modelling and Simulation Lab | | ***Code*** | VDM 351 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Core (PC) | | 02 | | 0 | 0 | 4 |
| ***Examination Duration (Hrs)*** | | ***Practical*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Electronics Devices and Circuits, Digital Electronics | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Understand** various semiconductor devices and circuit using simulators. |
| ***CO 2*** | **Compute** the characteristics of various digital and analog systems. |
| ***CO 3*** | **Analyse** Cadence, VTCAD, OrCAD and Xilinx tools for the implementation of digital and analog circuits. |
| ***CO 4*** | **Evaluate** various MOS devices performance using MATLAB and VTCAD. |

| ***Exp. No.*** | ***Name of the Experiment*** |
|---|---|
| ***1.*** | Study of Cadence tool for the implementation of Multistage Amplifier. |
| ***2.*** | Study of Cadence tool for the implementation of analog circuits (CS Amplifier). |
| ***3.*** | Implementation of a novel circuit and its performance analysis using Cadence tool (Flip-Flops using pass transistors). |
| ***4.*** | Design and simulation of CMOS (NMOS/PMOS) using VTCAD and their characteristics analysis. |
| ***5.*** | Design and simulation of Dual Gate MOSFET using VTCAD and their characteristics analysis. |
| ***6.*** | Design and simulation of Gate All Around FET (GAA-FET) using VTCAD and their characteristics analysis. |
| ***7.*** | Design and simulation of BJT using VTCAD and their characteristics analysis. |
| ***8.*** | Study of OrCAD tool for analysis of RC coupled amplifier. |
| ***9.*** | To plot the drain characteristics for n-channel MOSFET using MATLAB for implementation of MOSFET models in linear and saturation region. |
| ***10.*** | To plot the transfer characteristics for n-channel MOSFET in linear region and extract the various parameters (like threshold voltage ($V_{th}$), Transconductance ($g_m$), Mobility ($\mu$) and on-off current ratio ($I_{on}/I_{off}$) using MATLAB. |
| ***11.*** | To plot the transfer characteristics for n-channel MOSFET in saturation region and extract the various parameters (like threshold voltage ($V_{th}$), Transconductance ($g_m$), Mobility($\mu$) and on-off current ratio ($I_{on}/I_{off}$) using MATLAB. |
| ***12.*** | Write a program for the following condition using Xilinx.<br>Government wants to give subsidy to the citizens, so they decided that if income is greater than subsidy then income itself is the final income. Otherwise, subsidy will be added to income to get the total income. |
| **Innovative** | |
| ***13.*** | FPGA implementation of various logic gates in Xilinx tool. |
| ***14.*** | Design and Simulation of universal gates in VTCAD tool. |
| ***15.*** | Design and Simulation of Tri-Gate in VTCAD tool. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam |

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|---|---|---|---|---|---|---|
| *Master of Technology* | | | | | | |
| *VLSI Design and Systems* | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Advanced Nanotechnology | | ***Code*** | VDM 191 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE)(I) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basics of Physics and Chemistry | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Remember** the concepts of emerging world of nanoscience, Knowledge of single-electron devices and carbon based nanoelectronics devices. |
| ***CO 2*** | **Understand** the various top-down and bottom-up approaches for nanomaterial synthesis. |
| ***CO 3*** | **Apply** the acquired knowledge to develop novel nanomaterials. |
| ***CO 4*** | **Analyse** the properties of nanomaterials using various scanning probe techniques and spectroscopic techniques for material characterization. |
| ***CO 5*** | **Evaluate** the performance of nanotechnology related devices for various industrial applications. |
| ***CO 6*** | **Utilise** analytical tools in nanoscale engineering. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction to Nanotechnology:** Overview, Historical background, Importance of nanoscale, Bottom-up approaches, Top-down approaches, Functional approaches. | 8 |
| ***Unit 2:*** | **Nano Materials:** Fundamental concepts of nanomaterials, Allotropes of carbon, Graphene, Graphene nanoribbons, Fullerenes, Fullerites, Carbon nanotubes (CNTs), Bucky paper. | 8 |
| ***Unit 3:*** | **Nano Electronics:** Approaches to Nano electronics, Fabrication of integrated circuits, Introduction to microelectromechanical systems (MEMS), Nanoelectromechanical systems (NEMS), Nanowires, Nano-Circuits, Quantum wire, Quantum well. | 10 |
| ***Unit 4:*** | **Nano-Engineering Devices and Nano- Medicine:** Lab on chip, Micromachinery, Nanomotor, Nanopore, Nano sensor, Quantum point contact, Synthetic molecular motors, Medical applications of nanomaterials. | 8 |
| ***Unit 5:*** | **Analytical Tools in Nanoscale Engineering and Nanolithography:** Atomic force microscopy (AFM), Scanning tunnelling microscope (STM), Nanolithography: Dip-pen, Electron beam, Ion-beam sculpting, Nanoimprint lithograph, Photolithography. | 10 |
| **Total Hours** | | **44** |

| ***Textbooks*** |
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**Program Elective I**

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|---|---|
| **1.** | Shunri Oda, David Ferry, "***Nanoscale Silicon Devices***", CRC Press, Taylor & Francis Group, 1st Edition, 2016 |
| **2.** | Robert Puers, "***Nanoelectronics: Materials, Devices, Applications***", Wiley, 1st Edition 2017. |
| ***Reference Books*** | |
| **3.** | Suprio Datta, "***Lessons from nanoelectronics***", World Scientific publisher, 1st Edition, 2012. |
| **4.** | Gabriel M. Rebeiz, "***RF MEMS: Theory, Design, and Technology***", Wiley, 1st Edition, 2003. |
| **5.** | Julian W. Gardner, "***Microsensors, MEMS and Smart Devices***", Wiley, 1st Edition, 2002. |


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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Optimization Techniques in VLSI Design | | ***Code*** | VDM 192 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (I) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** VLSI Technology and Design | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Recall** the knowledge of modelling techniques based on incorporating empirical parameters. | | | | | |
| ***CO 2*** | **Understand** the performance parameters and yield estimation of optimization techniques. | | | | | |
| ***CO 3*** | **Apply** the knowledge of convex optimization techniques. | | | | | |
| ***CO 4*** | **Analyse** and **understand** Genetic algorithm in VLSI design. | | | | | |
| ***CO 5*** | **Assess** and **evaluate** FPGA for automatic test generation. | | | | | |
| ***CO 6*** | **Implement** optimization techniques in VLSI design. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Statistical Modelling:** Modelling sources of variations, Monte Carlo techniques, Process variation modelling- Pelgrom's model, Principal component-based modelling, Quad tree based modelling, Performance modelling-response Surface methodology, Delay modelling, Interconnect delay models. | 8 |
| ***Unit 2:*** | **Statistical Performance, Power and Yield Analysis:** Statistical timing analysis, Parameter space techniques, Bayesian networks leakage models, High level statistical analysis, Gate level statistical analysis, Dynamic power, Leakage power, Temperature and power supply variations, High level yield estimation and Gate level yield estimation. | 8 |
| ***Unit 3:*** | **Convex Optimization:** Convex sets, Convex functions, Geometric programming, Trade-off and sensitivity analysis, Generalized geometric programming, Geometric programming applied to digital circuit gate sizing, Floor planning, Wire sizing, Approximation and fitting- monomial fitting, Maxmonomial fitting, Posynomial fitting. | 9 |
| ***Unit 4:*** | **Genetic Algorithm:** Introduction, GA Technology-Steady state algorithm-Fitnessscaling-Inversion GA for VLSI design, Layout and test automation- Partitioning-automatic placement, Routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm taxonomy-multiway partitioning Hybrid Genetic-Encoding-Local Improvement-WDFR comparison of cas-standard cell placement-GASP algorithm-unified algorithm. | 9 |
| ***Unit 5:*** | **GA Routing Procedures and Power Estimation:** Global routing-FPGA technology mapping-circuit Generation-Test Generation in A GA framework-test generation procedure. Power | 8 |

| | | |
|---|---|---|
| | estimation-application of GA-standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs conventional algorithm. Hardware/Software Co-Designs. | |
| **Total Hours** | | **42** |

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| | ***Textbooks*** |
| **1.** | Ashish Srivastava, Dennis Sylvester, David Blaauwi, "***Statistical Analysis and Optimization for VLSI:Timing and Power***", Springer, 1st Edition, 2005. |
| **2.** | Kalyanmoy Dev, "***Optimization for Engineering Design: Algorithms and Examples***", PHI Learning, 2nd Edition, 2001. |
| | ***Reference Books*** |
| **3.** | PinakiMazumder, E. Mrudnick, "***Genetic Algorithm for VLSI Design, Layout and test Automation***", Prentice Hall, 1st Edition, 2002. |

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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Theory and Application of Embedded Systems | | ***Code*** | VDM 193 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (I) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Microcontrollers & Embedded Systems | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Recall** the basic concept of embedded system. | | | | | |
| ***CO 2*** | **Understand** the architecture and instruction sets of PIC microcontrollers. | | | | | |
| ***CO 3*** | **Relate** the knowledge of system firmware design. | | | | | |
| ***CO 4*** | **Analyse** structure of RTOS based embedded systems. | | | | | |
| ***CO 5*** | **Evaluate** ARM-32 bit processors as the advanced series microcontroller. | | | | | |
| ***CO 6*** | **Integrate** the concepts of advanced embedded systems for developing projects. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Embedded Systems:** Embedded vs General computing system, classification, application and purpose of Embedded system. Core of an Embedded System, Memory, Sensors, Actuators. Characteristics and quality attributes of embedded systems. | 8 |
| ***Unit 2:*** | **PIC Architectures:** PIC series of microcontrollers, Assembly basics, Instruction list and description, Addressing modes, Interrupts and timer. | 8 |
| ***Unit 3:*** | **System Firmware Design:** Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware. | 8 |
| ***Unit 4:*** | **RTOS Based Embedded System Design**: Basics of Operating systems, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling. | 8 |
| ***Unit 5:*** | **ARM-32 bit Microcontroller:** Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation. | 8 |
| **Total Hours** | | **40** |

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|---|---|
| | ***Textbooks*** |
| **1.** | Raj Kamal, "***Microcontrollers: Architecture, Programming, Interfacing and System Design***", Pearson Education India, 2nd Edition, 2005. |
| **2.** | J. Morton, "***The PIC Microcontroller***", Newnes, 3rd Edition, 2005. |
| | ***Reference Books*** |
| **3.** | A. Sloss, D. Symes, C. Wright, "***Arm System Developer's Guide: Designing and optimizing system software***", Morgan Kauffman Publisher, Illustrated edition, 2004. |
| **4.** | K. V. Shibhu, "***Introduction to Embedded Systems***", Tata McGraw Hill, 1st Edition, 2009. |
| **5.** | Frank Vahid, Tony Givargis, "***Embedded System Design, A Unified Hardware, Software Approach***", Wiley Publications, 3rd Edition, 1999. |

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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Digital Signal Processing for VLSI | | ***Code*** | VDM 194 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (I) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Digital Signal Processing | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the basic concepts of DFT- FFT in FIR filters and IIR filters. |
| ***CO 2*** | **Understand** iteration bound, pipelining and parallel processing. |
| ***CO 3*** | **Apply** the knowledge of retiming and parallel processing by using various fast convolution techniques. |
| ***CO 4*** | **Analyse** algorithmic strength reduction in filters transforms and pipelined and parallel recursive filters. |
| ***CO 5*** | **Evaluate** scaling and round off noise computation processes. |
| ***CO 6*** | **Design** and **develop** high-speed VLSI based devices. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction:**<br>Linear system theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR filters and IIR filters- Filter realizations. Representation of DSP algorithms-block diagram-SFG-DFG. | 8 |
| ***Unit 2:*** | **Iteration Bound:**<br>Data-Flow graph representations, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of multi-rate data-flow graph. Pipelining and parallel processing: Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power. | 8 |
| ***Unit 3:*** | **Retiming:**<br>Definitions-properties and problems- Solving systems of inequalities, Retiming techniques<br>**Fast Convolution:**<br>Cook-Toom algorithm, Winograd algorithm, Iterated convolution, Cyclic convolution, Design of fast convolution algorithm by inspection. | 8 |
| ***Unit 4:*** | **Algorithmic Strength Reduction in Filters and Transforms:**<br>Parallel FIR filters discrete cosine transform and Inverse DCT, Parallel architectures for rank order filters-odd even merge sort architecture, Rank order filter architecture, Parallel rank order filters-running order merge order sorter, Low power rank order filter.<br>**Pipelined and Parallel Recursive Filters:**<br>Pipeline interleaving in digital filters- Pipelining in 1st order IIR digital filters- Pipelining in higher-order IIR filters-clustered look ahead and stable clustered look ahead-parallel processing for IIR filters and problems. | 9 |
| ***Unit 5:*** | **Scaling and Round off Noise:** | 9 |

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|---|---|---|
| | Scaling and round off noise- State variable description of digital filters, Scaling and round off noise computation, Round off noise in pipelined IIR filters, Computation using state variable description, Slow-Down, Retiming and pipelining. | |
| **Total Hours** | | **42** |

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|---|---|
| ***Textbooks*** | |
| **1.** | K. K. Parhi, "***VLSI Digital Signal Processing*"**, John-Wiley, 1st Edition, 1999. |
| **2.** | John G. Proakis, Dimitris G. Manolakis, "***Digital Signal Processing***", Prentice Hall of India. 3rd Edition, 1996. |
| ***Reference Books*** | |
| **3.** | Richard J. Higgins, "***Digital signal processing in VLSI***", Prentice Hall, 1st Edition,1990. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Robust Control System | | ***Code*** | VDM 195 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (I) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Control Systems | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Explain** the motivation of robust control | | | | | |
| ***CO 2*** | **Compute** nominal stability and performance along with robust stability and performance | | | | | |
| ***CO 3*** | **Explain** robustness and uncertainty of systems | | | | | |
| ***CO 4*** | **Explain** robust stability and loop shaping | | | | | |
| ***CO 5*** | **Acquire** the fundamentals of H2 and H∞ control | | | | | |
| ***CO 6*** | **Design** feedback control systems | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction and Background**: Control System representations, System stabilities, Coprime factorisation and stabilising controllers, signals and systems norms. | 04 |
| ***Unit 2:*** | **Modeling of uncertain systems**: Introduction to concepts of model uncertainty, including both parametric and dynamic uncertainty, Linear fractional transformations and canonical forms. | 06 |
| ***Unit 3:*** | **Robustness Problems:** Linear fractional transformations and canonical forms. Performance measured via (induced) norms. Robust stability and performance problems. Solution of SISO robustness problems. | 06 |
| ***Unit 4:*** | **Computer-Aided Analysis Techniques**: Introduction to the structured singular value for robustness analysis of MIMO systems. Conversion of robustness problems to canonical M-Δ form. The small gain theorem and approximate computation of μ via efficient upper and lower bounds. Computer-aided tools for μ-analysis based on the Matlab Robust Control Toolbox. | 10 |
| ***Unit 5:*** | **Synthesis and Controller:** Design Optimal controller design including $H_2$ and $H_{infinity}$ optimal control. Scaled $H_{infinity}$-optimal control problems and μ-synthesis. Computer-aided tools to implement D,G-K iteration for advanced controller design. Lower order controllers: Absolute error approximation methods, reduction via fractional factors, relative error approximation methods, and frequency weighted approximation methods, Design case studies. | 10 |
| **Total Hours** | | **36** |

| ***Textbooks*** |
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## Program Elective I

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| | |
|---|---|
| **1.** | U. Mackenroth, "***Robust Control Systems-Theory and Case Studies"***, Springer International Edition, Springer, 2010 |
| **2.** | Kemin Zhou, "***Essentials of Robust Control"***, Prentice-Hall, 1st Edition, 1998 |
| **3.** | **Gu**, Da-Wei, **Petkov**, Petko, **Konstantinov**, Mihail M, "***Robust Control Design with MATLAB"***, Springer International Edition, Springer, 2009 |
| | ***Reference Books*** |
| **4.** | Richard.C.Dorf and R.T Bishop, "***Modern Control System"***, P.H.I |
| **5.** | S P Bhattacharya, L H Keel, H Chapellat, "***Robust Control: The Parametric Approach"***, Prentice-Hall, 1995 |
| **6.** | P C Chandrasekharan, "***Robust Control of Linear Dynamical Systems"***, Academic Press, 1996. |


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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | First | ***Subject Title*** | Control of Advanced Electric Machine | | ***Code*** | VDM 196 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (I) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Electrical Engineering | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Understand** the principle of operation and power converter for stepper motor |
| ***CO 2*** | **Understand** the principle of operation and power converter for switched and Synchronous reluctance motor |
| ***CO 3*** | **Understand** construction, principle of operation, theory of torque production in brushless DC motor |
| ***CO 4*** | **Explain** the control aspect of special electrical machines |
| ***CO 5*** | **Demonstrate** an understanding of the fundamental control practices associated with rotating machines |
| ***CO 6*** | **Summarize** the various performance characteristics of special electrical machines |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Stepper Motors -** Constructional features, principle of operation, modes of excitation, single phase stepping motors, torque production in variable Reluctance (VR) stepping motor, Dynamic characteristics, Drive systems and circuit for open loop control, Closed loop control of stepping motor, control of stepper motor using microcontroller. | 10 |
| ***Unit 2:*** | **Switched Reluctance Motors -** Constructional features, principle of operation. Torque equation, Power controllers, Characteristics and control. Microprocessor based controller. Sensor less control. | 8 |
| ***Unit 3:*** | **Synchronous Reluctance Motors-Constructional features:** axial and radial air gap Motors. Operating principle, reluctance torque – Phasor diagram, motor characteristics. | 8 |
| ***Unit 4:*** | **Permanent Magnet Brushless DC Motors -** Commutation in DC motors, Difference between mechanical and electronic commutators, Hall sensors, Optical sensors, Multiphase Brushless motor, Square wave permanent magnet brushless motor drives, Torque and EMF equation, Torque-speed characteristics, Controllers-Microprocessor based controller. Sensorless control. | 10 |
| **Total Hours** | | **36** |

| ***Textbooks and Reference Books*** | |
|---|---|
| **1.** | Kenjo T., Sugawara A, "***Stepping Motors and their Microprocessor Control***", Clarendon Press, Oxford, 1st Edition, 1994 |

**Program Elective I**

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| **2.** | Miller T. J. E., "***Switched Reluctance Motor and Their Control"***, Clarendon Press, Oxford, 1st Edition, 1993. |
| **3.** | Miller T. J. E., ***Brushless Permanent Magnet and Reluctance Motor Drives***, Clarendon Press, Oxford, 2nd Edition, 1989. |
| **4.** | B K Bose, ***Modern Power Electronics & AC drives***, Pearson, 1st Edition, 2002. |


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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Micro-Sensors and MEMS | | ***Code*** | VDM 291 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (II) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** VLSI Technology | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Recall** the basic principles of different sensors and actuators. | | | | | |
| ***CO 2*** | **Understand** the process of miniaturization of a sensor and actuator to produce a micro sensor and micro actuator and its integration with microelectronics circuitry. | | | | | |
| ***CO 3*** | **Apply** various fabrication technologies for miniaturization of sensors and actuators for MEMS. | | | | | |
| ***CO 4*** | **Analyze** the different properties of sensors and actuators. | | | | | |
| ***CO 5*** | **Evaluate** the behaviour of MEMS devices. | | | | | |
| ***CO 6*** | **Create** approaches for the designing of different MEMS based devices for various real-life applications. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Microfabrication and Micromachining:** Integrated circuit processes, Bulk micromachining, Isotropic etching and anisotropic etching, Wafer bonding, High aspect-ratio processes (LIGA). | 10 |
| ***Unit 2:*** | **Physical Micro-Sensors:** Classification of physical sensors, Integrated, Intelligent, Smart sensors, Sensor principles and examples: Thermal sensors, Electrical sensors, Mechanical sensors, Chemical and biosensors. | 8 |
| ***Unit 3:*** | **Micro actuators:** Electromagnetic and thermal micro-actuation, Mechanical design of micro actuators, Micro actuator examples, Microvalves,Micropumps, Micromotors Micro actuator systems, Success stories, Ink-Jet printer heads, Micro-Mirror TV projector. | 8 |
| ***Unit 4:*** | **Surface Micromachining:** One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon dioxide, Silicon nitride, Piezoelectric materials, Surface micromachined systems: Success stories, Micromotors, Gear trains mechanisms. | 8 |
| ***Unit 5:*** | **Application Areas:** All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices E.G. DNA-chip, Micro-arrays. MEMS for RF applications: Need for RF MEMS components in communications, Space and defence applications. | 8 |
| **Total Hours** | | **42** |

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|---|---|
| | ***Textbooks*** |
| **1.** | Chang Liu, "***Foundations of MEMS***", Pearson, 2nd Edition, 2012. |
| **2.** | Rai - Choudhury P., "***MEMS and MOEMS Technology and Applications***", PHI Learning Private Limited, 1st Edition, 2009. |
| **3.** | Julian W. Gardner, "***Microsensors, MEMS and Smart Devices"***, Wiley, 1st Edition, 2002. |
| | ***Reference Books*** |
| **4.** | Gabriel M. Rebeiz, "***RF MEMS: Theory, Design, and Technology***", Wiley, 1st Edition, 2003. |
| **5.** | Stephen D. Senturia, "***Microsystem design***", Springer, 1st Edition, 2006. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | RF Microelectronics Devices | | ***Code*** | VDM 292 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (II) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Electronics Devices and Circuits, Microwave Engineering, | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the concepts of wireless technology in RF design: |
| ***CO 2*** | **Understand** the modulation techniques for RF circuits. |
| ***CO 3*** | **Apply** the basics of detectors and transistor modelling, Mobile RF communication systems and basics of multiple access techniques. |
| ***CO 4*** | **Analyse** the concept of BJT and MOSFET behaviour at RF frequencies. |
| ***CO 5*** | **Assess** and evaluate Radio frequency devices. |
| ***CO 6*** | **Design** and **develop** RF based microelectronic devices. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction:** Introduction to RF and wireless technology: Complexity, Design and applications, Choice of technology. Basic concepts in RF design, Nonlinearly and time variance, Random processes and noise. | 8 |
| ***Unit 2:*** | **Modulation Techniques for RF Circuits:** Definition of sensitivity, Dynamic range, Conversion gains and distortion. Analog and Digital modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and non-coherent detection. | 10 |
| ***Unit 3:*** | **Detectors and Transistor Modelling:** Mobile RF communication systems and basics of multiple access techniques. Receiver and transmitter architectures and testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct conversion and two steps transmitters. BJT and MOSFET behaviour at RF frequencies, Modelling of the transistors and SPICE models. | 8 |
| ***Unit 4:*** | **Mixers and Oscillators:** Noise performance and limitation of devices. Integrated parasitic elements at high frequencies and their monolithic implementation. Basic blocks in RF systems and their VLSI implementation: Low noise amplifiers design in various technologies, Design of mixers at GHz frequency range. Various mixers, Their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-power trade-off. Resonator less VCO design. Quadrature and single-sideband generators. | 8 |
| ***Unit 5:*** | **RF Synthesizer:** Radio frequency synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power amplifiers design. Linearization techniques, | 8 |

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| | | |
|---|---|---|
| | Design issues in integrated RF filters. Some discussion on available CAD tools for RF VLSI designs. | |
| **Total Hours** | | **42** |

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|---|---|
| | ***Textbooks*** |
| **1.** | B. Razavi, "***RF Microelectronics***", Prentice-Hall PTR, 2nd Edition, 2012. |
| **2.** | T. H. Lee, "***The Design of CMOS Radio-Frequency Integrated Circuits***", Cambridge University Press, 1st Edition, 1998. |
| | ***Reference Books*** |
| **3.** | R. Jacob Baker, H. W. Li, and D.E. Boyce, "***CMOS circuit design, Layout and simulation***", Prentice-Hall of India, 1st Edition, 1998. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | VLSI Circuits for Biomedical Application | | ***Code*** | VDM 293 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (II) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Advanced VLSI Circuit Design, CMOS Analog Circuit Design | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the concepts of neurochemical and neuro potential devices. |
| ***CO 2*** | **Understand** the mechanisms involved in the design of CMOS circuits for implantable biomedical devices and wireless biomedical applications. |
| ***CO 3*** | **Analyse** CMOS circuits for wireless medical application. |
| ***CO 4*** | **Apply** microneedles and their interfacing with neural systems. |
| ***CO 5*** | **Evaluate** the process of neuro-signal acquisition and amplification, neurochemical signal recording, and neurostimulation. |
| ***CO 6*** | **Develop** CMOS circuits for biomedical applications. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction:** Wireless integrated neurochemical and neuropotential circuits: Introduction, Neurochemical sensing, Neuropotential sensing, RF telemetry and power harvesting in implanted devices, Multimodal electrical and chemical sensing. Visual cortical neuroprosthesis: A system approach: Introduction, System architecture, Prosthesis exterior body unit and wireless link, Body implantable unit, System prototype. | 9 |
| ***Unit 2:*** | **CMOS Circuits for Biomedical Implantable Devices:** Introduction, Inductive link to deliver power to implants, High data rate transmission through inductive links, Energy and bandwidth issues in multi-channel bio-potential recording. Towards self –powered sensors and circuits for biomedical implants: Introduction, Stress, Strain and fatigue predication, In vivo strain measurement and motivation. Fundamental of piezoelectric-transduction and power delivery, Sub-microwatt piezo-powered VLSI circuits. | 9 |
| ***Unit 3:*** | **CMOS Circuits for Wireless Medical Application:** Introduction, Spectrum regulations for medical use, Integrated receiver and transmitter architecture, Radio architecture, System budget, Low noise amplifier, Mixer, Polyphase filter, Power amplifier, PLL. Error correcting codes for in vivo RF wireless links. | 8 |
| ***Unit 4:*** | **Microneedles:** Introduction, Fabrication methods for hollow out –of –plane microneedles, Application for microneedles. Integrated circuit for neural interfacing: Introduction, nature of neural signals, Neural signal amplification. | 8 |
| ***Unit 5:*** | **Integrated Circuits for Neural Applications:** | 8 |

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|---|---|---|
| | Integrated circuit for neural interfacing (Neurochemical recording), Integrated circuit for neural interfacing (Neural Stimulation): Introduction, Electrode configuration and tissue volume conductor, Electrode- Electrolyte Interface, Efficacy, Stimulus generator, Stimulation front end circuits. | |
| **Total Hours** | | **42** |

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|---|---|
| | ***Textbooks*** |
| **1.** | Kris Iniewski, "***VLSI Circuit Design for Biomedical Application***", Artech House Publishers, 1st Edition, 2008. |
| **2.** | D. A. Hodges, H. G. Jackson and R. A. Saleh, "***Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology***", Tata McGraw-Hill, 3rd Edition, 2003. |
| | ***Reference Books*** |
| **3.** | Parag. K. Lala, "***Digital circuit testing and testability***", Academic Press, 1st Edition, 1997. |
| **4.** | Ashok K. Sharma, "***Semiconductor memories technology, testing and reliability***", Prentice-Hall of India Private Limited, 1st Edition, 2002. |

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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Microwave & MM-wave Integrated Circuits and Applications | | ***Code*** | VDM 294 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (II) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Microwave Engineering | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Describe** the requirement of MMIC and MM-wave technologies and their various applications. | | | | | |
| ***CO 2*** | **Understand** the fabrication processes Circuit of Microwave Integrated MIC. | | | | | |
| ***CO 3*** | **Implement** the various active and passive circuit elements for microwave and MM-wave technology. | | | | | |
| ***CO 4*** | **Analyse** the various measurement systems using MM-wave technology. | | | | | |
| ***CO 5*** | **Evaluate** the microwave components for designing microwave Integrated circuits. | | | | | |
| ***CO 6*** | **Design** of MMIC using MM-Wave Technology. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction**:<br>Introduction to Monolithic Microwave Integrated Circuits (MMICs) technology, different types of MMIC, Advantages disadvantages and application of MMICs, MMIC fabrication techniques, Thick and thin film technologies and materials, Encapsulation and mounting of active devices, Introduction to MM-wave integrated circuits, GaAs fabrication technology and various processes, Materials used for MM-wave integrated guides. | 10 |
| ***Unit 2:*** | **Passive components:**<br>Introduction, Inductors, Capacitors, Resistors, Via-holes, and grounding, Microstrip components, Coplanar circuits, Multilayer techniques, Micromachined passive components. | 8 |
| ***Unit 3:*** | **Active Semiconductor circuit elements:**<br>Active device technologies and design approaches, Fabrication and modeling: Bipolar junction transistor, Hetero junction bipolar transistor, High electron mobility transistor, MESFET, CMOS, BiCMOS. | 10 |
| ***Unit 4:*** | **Measurement Techniques:**<br>Introduction, Test fixture measurements, Probe station measurements, Thermal and cryogenic measurements, Experimental field probing techniques, MM-wave measurement techniques: Electric field probe, Measurement of attenuation constant and guide wavelength. Measurement at radiation loss at bents. | 8 |
| ***Unit 5:*** | **System Application:**<br>MICs in phased array radars, MICs in satellite television systems, Microwave radio systems, Monolithic MM-wave transceiver. | 6 |

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|---|---|
| **Total Hours** | **42** |

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| | ***Textbooks*** |
| **1.** | I. D. Robertson and S. Lucyszyn, "***RFIC and MMIC design and technology***", The Institute of Electrical Engineers, 2nd Edition 2001. |
| **2.** | Leo G. Maloratsk, "***Passive RF and Microwave Integrated Circuits***", Elsevier, 1st Edition, 2004. |
| **3.** | K. C. Gupta and A. Singh, "***Microwave Integrated circuit***", John Wiley & Sons, 2nd Edition, 1974 |
| **4.** | E. Carey and S. Lidholm, "***Millimeter wave Integrated Circuit***", Springer, 2nd Edition, 2005 |
| | ***Reference Books*** |
| **5.** | I. Kneppo, J. Fabian, P. Bezousek, P. Hrnicko and M. Pavel, "***Microwave Integrated Circuits***", 1st Edition, Springer. |
| **6.** | S. K. Koul, "***Millimeter Wave and Optical Dielectric Integrated Guides and Circuits***", John Wiley & Sons, 1st Edition, 1997. |
| **7.** | Duixian Liu, Ulrich Pfeiffer, Janusz Grzyb and Brian Gaucher, "***Advanced Millimeter-wave Technologies: Antennas, Packaging and Circuits***", Wiley, 1st Edition, 2009. |

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|---|---|
| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Renewable Energy Resources and Energy Management | | ***Code*** | VDM 295 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (II) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Physics | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Describe** the knowledge of Solar Power Generation and solar thermal applications. | | | | | |
| ***CO 2*** | **Illustrate** the photovoltaic characteristics, classifications, fuel cells and wind energy systems. | | | | | |
| ***CO 3*** | **Demonstrate** the Geothermal energy for conversion in electrical energy. | | | | | |
| ***CO 4*** | **Analyse** the performance analysis of Fuel cell and MHD. | | | | | |
| ***CO 5*** | **Evaluate** the various renewable power generation techniques and compare the results. | | | | | |
| ***CO 6*** | **Develop** solar panels, fuel cells and wind energy techniques. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Solar Thermal Energy:** Solar radiation flat plant collectors and their materials, application and performance, focusing of collectors and their materials, applications and performance solar thermal power plants, thermal energy storage for solar heating and cooling, limitations . | 08 |
| ***Unit 2:*** | **Photo voltaic System-**Solar cell characteristics, solar cell classifications, solar cell module, panel and Array constructions, Maximizing solar PV output and Load Matching, Maximum Power Point Tracking (MPPT), Balance of system components, Solar PV applications | 08 |
| ***Unit 3:*** | **Fuel Cells:** Principle of working of various types of fuel cells and their working, performance and limitations.<br>**Thermo-electrical and thermionic Conversions:** Principle of working, performance and limitations | 06 |
| ***Unit 4:*** | **Wind Energy:** Wind power and its sources, site selection, criterion , momentum theory, classification of rotors , concentrations and augments, wind characteristics . performance and limitations of energy conversion systems. | 06 |
| ***Unit 5:*** | **Geothermal Energy:** Resources of geothermal energy, thermodynamics of geo-thermal energy conversion-electrical conversion, non-electrical conversion, environmental considerations.<br>**Magneto-hydrodynamics (M H D):** Principle of working of M H D Power plant, performance and limitations.<br>**Bio-mass:** Availability of bio-mass and its convention theory . | 08 |
| **Total Hours** | | **36** |

| ***Textbooks*** |
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## Program Elective II

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|---|---|
| **1.** | B.H Khan, "***Non-Conventional Energy Resources***" Tata McGraw-Hill Education 2nd Edition |
| **2.** | Max Kurtz , "**Handbook of Engineering Economics: Guide for Engineers, Technicians, Scientists, and Managers",** McGraw-Hill, 1st Edition, 1984 |
| **3.** | A. Mani , "***Handbook of solar radiation Data for India*** ." Allied Publishers Pvt. Ltd., 1st Edition, 1980. |
| **4.** | Peter Auer , "***Advances in Energy System and Technology*** ", Vol. I & II Edited by Academic Press, 1st Edition, |
| **5.** | F.R. the MITTRE , "***Wind Machines" by Energy Resources and Environmental Series".*** Van Nostrand Reinhold Inc.,U.S.; 2nd Revised Edition, 1980 |
| | ***Reference Books*** |
| **6.** | Frank Kreith , "***Solar Energy Hand Book",*** |
| **7.** | N. Chermisinogg and Thomes , C. Reign , "***Principles and Application of solar Energy*** ". TMH, 2nd Edition, 1980. |


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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Second | ***Subject Title*** | Multivariable Control Systems | | ***Code*** | VDM 296 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (II) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Electrical Engineering | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the used of classical control in multivariable systems |
| ***CO 2*** | **Extend** the basic knowledge and understanding of the multivariable systems |
| ***CO 3*** | **Implement** the multivariable systems through open and closed loop transfer function and study of their behaviour. |
| ***CO 4*** | **Analyze** a multivariable dynamic system |
| ***CO 5*** | **Evaluate** the stability, performance and robustness of a closed-loop system |
| ***CO 6*** | **Design** an appropriate controller for the multivariable system |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction to Multi-variable systems: -** Classical feedback control in the multivariable case, Introduction to multivariable control, Elements of linear systems theory, Limitations on performance in SISO and MIMO systems. | 6 |
| ***Unit 2:*** | **Analysis of Multi-Variable System:-**Open loop dynamic analysis in state space, Multi-variable transfer function, Multi variable pole – zero concept, quantitative measure of singularity, closed loop dynamic analysis. | 8 |
| ***Unit 3:*** | **Multi – Single loop designs:-**Preliminary consideration of interaction analysis and loop pairing, the relative gain array, loop pairing using RGA, loop pairing of nonlinear system, loop pairing for system with pure integrator modes, loop pairing for non-square systems, multi-loop controller, controller tuning for multi-loop system. | 8 |
| ***Unit 4:*** | **Introduction to De-couplers:-**Introduction, Decoupling, feasibility of steady state de-coupler design, steady state decoupling by singular value decomposition. | 6 |
| ***Unit 5:*** | **Design of multivariable systems**:- Multi-loop controller Design procedure, Controller tuning for multi-loop system, Multivariable controller design. | 6 |
| **Total Hours** | | **34** |

| ***Textbooks*** | |
|---|---|
| **1.** | Y. S. Apte, ***Linear multivariable control system***, Tata McGraw Hill, 1st Edition, 1981 |

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| **2.** | Dale E. Seborg, Thomas F. Edgar, and Duncan A. Mellichamp, ***Process Dynamics and Control***,Wiley India, 1st Edition, 2003. |
| | ***Reference Books*** |
| **3.** | C. T. Chen, ***Linear system theory and design***, Oxford University Press, 1999. |
| **4.** | John Bay, ***Fundamentals of linear state space systems***, Tata McGraw Hill, 1998. |
| **5.** | Wilson Rugh, ***Linear system theory***, Prentice Hall, 1996. |


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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | Organic Electronics Devices and Circuits | | ***Code*** | VDM 391 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (III) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Electronics Engineering, Electronics Devices and Circuits. | | | | | | |
| ***Course Outcomes*** | | | | | | |
| **Upon completion of this course, the students will be able to** | | | | | | |
| ***CO 1*** | **Ability** to describe basic concepts and limitations of conventional silicon-based semiconductor devices. | | | | | |
| ***CO 2*** | **Understand** the basic concepts and classification of organic materials. | | | | | |
| ***CO 3*** | **Apply** the advancement of charge transport in organic materials for different organic electronic devices. | | | | | |
| ***CO 4*** | **Design** and **develop** innovative organic electronic devices. | | | | | |
| ***CO 5*** | **Evaluate** the performance of organic solar cells. | | | | | |
| ***CO 6*** | **Analyse** the different properties of OLED. | | | | | |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Organic Materials and Device Physics:** Introduction; Organic materials: Conducting polymers and small molecules, Organic semiconductors: p-type and n-type semiconductors, Source, Drain and Gate electrodes, Gate dielectrics, Substrate. Energy band diagram and concept of charge transport in organic semiconductors; Comparison between organic and inorganic semiconductors including the merits, Demerits and limitations. | 9 |
| ***Unit 2:*** | **Organic Thin Film Transistors (OTFTs):** Introduction; Operating principle; Output and transfer characteristics; Classification of various organic thin film transistors (OTFT) structures; Performance parameters; Impact of structural parameters on behaviour of OTFT; Concept of contact resistance; Single Gate (SG) and Dual Gate (DG) TFT performance comparison; Merits, Demerits, Limitations and future scope. Applications: - Organic complementary inverter circuits; Organic memory - Organic static random-access memory (OSRAM). | 10 |
| ***Unit 3:*** | **Organic Light Emitting Diodes (OLEDs)** Introduction; Organic materials for OLEDs; Classification of OLEDs, Operating principle; Output and transfer characteristics; Analysis of OLED performance: Optical, Electrical and thermal properties, Merits and demerits; Stability issues; OLEDs as display applications. | 8 |
| ***Unit 4:*** | **Organic Solar Cell:** Introduction; Operating principle; Characteristics; Materials for organic solar cells; Classification of organic solar cell- Single layer, Bi-layer and bulk hetero junction organic solar cell; Merits and demerits; Applications and future scope. | 7 |
| ***Unit 5:*** | **Organic Sensors:** | 8 |

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|---|---|---|
| | Introduction; Working principle and organic sensing materials for pressure sensors (Piezoresistive, Piezoelectric, and Capacitive sensor), Temperature sensors, Humidity sensors and pH sensor; comparison between organic and conventional sensors including merits, demerits and limitations; Applications of organic sensors; Basics of ionic polymer–metal composites (IPMC) and its applications. | |
| **Total Hours** | | **42** |

| | |
|---|---|
| | ***Textbooks*** |
| **1.** | Hagen Klauk, "***Organic Electronics: Materials, Manufacturing and Applications***", Wiley-VCH VerlagGmbh& Co. KGaA, Germany, 1st Edition, 2006. |
| **2.** | Klaus Mullen, UllrichScherf, "***Organic Light Emitting Devices: Synthesis, Properties and Applications***", Wiley-VCH VerlagGmbh& Co. KGaA, Germany, 1st Edition, 2005. |
| **3.** | Johannes Karl Fink, "***Polymeric Sensors and Actuators***", John Wiley & Sons, 1st Edition, 2012. |
| | ***Reference Books*** |
| **4.** | Hagen Klauk, "***Organic Electronics II: More Materials and Applications***", Wiley-VCH VerlagGmbh& Co. KGaA, Weinheim, Germany, 1st Edition, 2012 |
| **5.** | Flora Li, Arokia Nathan, Yiliang Wu, Beng S. Ong, "***Organic Thin Film Transistor Integration: A Hybrid Approach***", Wiley-VCH, Germany; 1st Edition, 2011. |
| **6.** | Wolfgang Brutting, "***Physics of Organic Semiconductors***", Wiley-VCH VerlagGmbh& Co. KGaA, Germany, 2nd Edition, 2005. |
| **7.** | Daniel A. Bernards, Róisín M. Owens, George G. Malliaras, "***Organic Semiconductors in Sensor Applications***", Springer Science & Business Media, 1st Edition, 2008. |

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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| *Department of Electronics and Communication Engineering* | | | | | | |
|---|---|---|---|---|---|---|
| *Master of Technology* | | | | | | |
| *VLSI Design and Systems* | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | Memory Design and Testing | | ***Code*** | VDM 392 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (III) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Low Power VLSI Design | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Acquire** the fundamental knowledge of CMOS memory devices. |
| ***CO 2*** | **Infer** about configuration of fundamental VLSI chip. |
| ***CO 3*** | **Ability** to implement high performance digital VLSI memory systems. |
| ***CO 4*** | **Analyse** different techniques required to implement low power memory chip. |
| ***CO 5*** | **Evaluate** the characteristics digital VLSI memory systems. |
| ***CO 6*** | **Design** of low power memory devices. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction to Memory Chip Design:** Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology. | 10 |
| ***Unit 2:*** | **Basics of RAM Design and Technology:** Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law. **On-Chip Voltage Generators:** Substrate-Bias Voltage (VBB) Generator, Voltage Up Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators. | 8 |
| ***Unit 3:*** | **DRAM Circuits:** High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources. | 8 |
| ***Unit 4:*** | **High-Performance Subsystem Memories:** Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM | 8 |

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|---|---|---|
| | Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits. | |
| ***Unit 5:*** | **Ultra-Low-Voltage Memory Circuits:** Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits. | 8 |
| **Total Hours** | | **42** |

| | |
|---|---|
| | ***Textbooks*** |
| **1.** | Itoh, K., ***VLSI Memory Chip Design***, Springer, 1st Edition, 2006. |
| **2.** | Sharma, A. K., ***Semiconductor Memories: Technology, Testing and Reliability***, Wiley- IEEE press, 1st Edition, 2002. |
| | ***Reference Books*** |
| **3.** | J. B. Kuo and J. H. Lou, Low "***Voltage CMOS VLSI Circuits***", Wiley, 1st Edition, 1999. |
| **4.** | J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, "***Digital Integrated Circuits: A Design Perspective***", 2nd Edition, Pearson, 2003. |

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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | System on Chip Design and Testing | | ***Code*** | VDM 393 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (III) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** VLSI Technology | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the concepts of System-on-Chip (SoC) Testing. |
| ***CO 2*** | **Understand** the concepts of digital test architectures design. |
| ***CO 3*** | **Apply** the concepts of SoC on delay testing and low-power testing. |
| ***CO 4*** | **Analyse** the basics of system/network-on-chip test architectures. |
| ***CO 5*** | **Assess** and **evaluate** debug and diagnosis. |
| ***CO 6*** | **Implement** different testing techniques in SoC. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction:**<br>Importance of system-on-chip testing, Basics of SoC testing, Basics of memory testing, SoC design examples.<br>**Digital Test Architectures:**<br>Scan design, Logic built-In self-test, Test compression, Random-access scan design.<br>**Fault-Tolerant Design:**<br>Fundamentals of fault tolerance, Fundamentals of coding theory, Fault tolerance schemes | 8 |
| ***Unit 2:*** | **System/Network-on-Chip Test Architectures:**<br>System-on-Chip (SoC) testing, Network-on-Chip (NoC) testing, Design and test practice: Case studies.<br>**SIP Test Architectures:**<br>Introduction, Bare die, Functional system test, Test of embedded components.<br>**Delay Testing:**<br>Delay test application, Delay fault models, Delay test sensitization, Delay fault, Delay fault test generation, Pseudo-functional testing to avoid over-testing | 8 |
| ***Unit 3:*** | **Low-Power Testing:**<br>Introduction, Energy and power modelling, Test power issues, Low-power scan testing, Low-power built-in self-test, Low-power test data compression, Low-power RAM testing.<br>**Coping with Physical Failures, Soft Errors, and Reliability Issues:**<br>Signal integrity, Manufacturing defects, Process variations, and Reliability, Soft errors, Defect and error tolerance. | 8 |
| ***Unit 4:*** | **Design for Manufacturability and Yield:** | 8 |

| | | |
|---|---|---|
| | Introduction, Yield, components of yield, Photolithography, DFM and DFY, Variability, Metrics for DFX.<br>**Design for Debug and Diagnosis:**<br>Introductiontologic design for debug and diagnosis (DFD) structures, Probing technologies, Circuit editing, Physical DFD structures, Diagnosis and debug process. | |
| ***Unit 5:*** | **Software-Based Self-Testing:**<br>Introduction, Software-based self-testing paradigm, Processor functional fault self-testing, Processor structural fault self-testing, Processor self-diagnosis, testing global interconnect, testing nonprogrammable cores, Instruction-level DFT, DSP-Based Analog/Mixed-signal component testing.<br>**Field Programmable Gate Array Testing:**<br>Overview of FPGAs, Testing approaches, BIST of programmable resources, Embedded processor-based testing | 10 |
| **Total Hours** | | **42** |

| | |
|---|---|
| | ***Textbooks*** |
| **1.** | Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "***System-On-Chip Test Architectures (Nanometer Design for Testability)***", Elsevier, 1st Edition, 2008. |
| | ***Reference Books*** |
| **2.** | Erik Larsson, "***Introduction to Advanced system- on- chip test design and optimization***", Springer, 5th Edition, 2006. |

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| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |

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| ***Department of Electronics and Communication Engineering*** | | | | | | |
|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | VLSI Physical Design Automation | | ***Code*** | VDM 394 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (III) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Digital VLSI Circuit Design | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Recall** the concepts of VLSI design automation tools. |
| ***CO 2*** | **Understand** different layout compaction, placement, and routing algorithms. |
| ***CO 3*** | **Apply** the concepts of Logic Synthesis in VLSI design. |
| ***CO 4*** | **Analyse** floor planning and routing algorithms. |
| ***CO 5*** | **Assess** and **evaluate** scheduling algorithms, allocation, and assignment. |
| ***CO 6*** | **Optimize** design layouts for floor-planning, placement, and routing. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **VLSI Design Automation Tools:** Design cycle, Design styles, Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools. | 10 |
| ***Unit 2:*** | **Layout Compaction, Placement and Routing:** Design rules, Symbolic layout, Applications of compaction, Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms. | 8 |
| ***Unit 3:*** | **Floor Planning and Routing:** Floor planning concepts, Shape functions and Floor planning, Sizing, Local routing, Area routing, Channel routing, Global routing and its algorithms. | 8 |
| ***Unit 4:*** | **Simulation and Logic Synthesis:** Gate level and switch level modelling and simulation. Introduction to combinational logic synthesis, ROBDD principles, Implementation, Construction and manipulation, Logic synthesis. | 8 |
| ***Unit 5:*** | **High-Level Synthesis:** Hardware model for high level synthesis, Internal representation of input algorithms, Allocation, Assignment and scheduling, Scheduling algorithms. Aspects of assignment. | 8 |
| **Total Hours** | | **42** |

| ***Textbooks*** | |
|---|---|
| **1.** | S. H. Gerez, "***Algorithms for VLSI Design Automation***", John Wiley, 3rd Edition, 2000. |
| **2.** | N. A. Sherwani, "***Algorithms for VLSI Physical Design Automation***", Kluwer, 3rd edition, 1999. |

## Program Elective III

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| | ***Reference Books*** |
|---|---|
| **3.** | M. Sait, H. Youssef, "***VLSI Physical Design Automation***", World scientific, 1st Edition, 1999. |
| **4.** | M. Sarrafzadeh, "***Introduction to VLSI Physical Design***", McGraw Hill (IE), student Edition, 1996. |

| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |
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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | Power Quality Assessment | | ***Code*** | VDM 395 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (III) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Electrical Engineering | | | | | | |

***Course Outcomes***

**Upon completion of this course, the students will be able to**

| | |
|---|---|
| ***CO 1*** | **Describe** the characteristics of ac transmission system, shunt and series reactive compensation. |
| ***CO 2*** | **Understand** waveform distortion and processing techniques, and their power assessment concepts. |
| ***CO 3*** | **Demonstrate** the working principles of FACTS devices and their operating characteristics. |
| ***CO 4*** | **Analyse** Static synchronous Compensator **(**STATCOM). |
| ***CO 5*** | **Estimate** the working principles of devices to improve power quality. |
| ***CO 6*** | **Propose** the power quality monitoring system and their harmonic analysis. |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Introduction:** **P**ower quality-voltage quality-overview of power quality phenomena-classification of power quality issues-power quality measures and standards-THD-TIF-DIN-message weights-flicker factor-transient phenomena-occurrence of power quality problems-power acceptability curves-IEEE guides, EMC standards and recommended practices. | 8 |
| ***Unit 2:*** | **Power Assessment under Waveform Distortion & Processing Techniques:** Introduction, single phase definitions, three phase definitions, illustrative examples, Fundamental frequency characterization, Fourier analysis, Fast Fourier Transform, Window functions, Efficiency of FFT algorithms, alternative transforms, wavelet transform, Hartely transform, Automation of disturbance recognition. | 8 |
| ***Unit 3:*** | **Power Quality Monitoring:** Introduction, transducers, CT, PT, power quality instrumentation, Harmonic monitoring, event recording, flicker monitoring, assessment of voltage and current unbalance, examples of application | 6 |
| ***Unit 4:*** | **Evaluation of power system harmonic distortion:** Introduction, direct harmonic analysis, incorporation of harmonic voltage sources, derivation of network harmonic impedances, solution by direct injection, Representation of individual power system components, implementation of harmonic analysis, post processing and display of results. | 6 |
| ***Unit 5:*** | **Harmonic Mitigation & Grounding:** Passive filtering, Harmonic resonance, Impedance Scan Analysis-Active Power Factor Corrected Single Phase Front End, introduction to three Phase | 8 |

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| | | |
|---|---|---|
| | APFC and Control Techniques, Grounding and wiring–introduction-NEC grounding requirements-reasons for grounding-typical grounding and wiring problems-solutions to grounding and wiring problems. | |
| **Total Hours** | | **36** |

| ***Textbooks and Reference Books*** | |
|---|---|
| **1.** | Math H. Bollen ***,"Understanding Power Quality Problems***", Wiley-IEEE Press; 1st Edition, 1999. |
| **2.** | G. T. Heydt Stars "***Electric Power Quality"*** , Circle Publishers, 2nd Edition, 1994. |
| **3.** | J. Arrillaga, "***Power System Quality Assessment"***. John Wiley, 2nd Edition, 2000. |
| **4.** | Surya Santoso, H. Wayne Beaty, Roger C. Dugan, Mark F. McGranaghan, "***Electrical Power System Quality***", McGraw Hills, 2nd Edition, 2002. |

| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |
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|---|---|---|---|---|---|---|
| ***Master of Technology*** | | | | | | |
| ***VLSI Design and Systems*** | | | | | | |
| ***Semester*** | Third | ***Subject Title*** | Optimal & Adaptive Control | | ***Code*** | VDM 396 |
| ***Course Components*** | | ***Credits*** | ***Contact Hours*** | ***L*** | ***T*** | ***P*** |
| Program Elective (PE) (III) | | 03 | | 3 | 0 | 0 |
| ***Examination Duration (Hrs)*** | | ***Theory*** | ***Weightage: Evaluation*** | ***CWA*** | ***MSE*** | ***ESE*** |
| | | 03 | | 25 | 25 | 50 |
| ***Pre-requisite:*** Basic Electrical Engineering | | | | | | |

| ***Course Outcomes*** | |
|---|---|
| **Upon completion of this course, the students will be able to** | |
| ***CO 1*** | **Describe** performance index and to define various optimal control problems |
| ***CO 2*** | **Extend** knowledge of discrete linear regulator problem using dynamic programming |
| ***CO 3*** | **Apply** the conditions for optimality and to solve continuous time linear regulator problem |
| ***CO 4*** | **Examine** minimum time and minimum control effort problems |
| ***CO 5*** | **Evaluate** adaptive control problem and to learn the mathematical description of model reference adaptive systems |
| ***CO 6*** | **Design** adaptive systems using various techniques |

| ***Unit No.*** | ***Content*** | ***Hours*** |
|---|---|---|
| ***Unit 1:*** | **Problem Formulation**: Mathematical model, Physical constraints, Characteristics of the plants, Performance Measure, optimal control problems, selection of performance measure, state regulator problem, output regulator problem.<br>**Calculus of Variations**: Fundamental concepts, minimization of functions, minimization of Functionals, Lagrange multiplier approach, constrained extrema, Variational approach to optimal control problems, formulation of variational calculus using Hamiltonian Method. | 08 |
| ***Unit 2:*** | **Dynamic Programming**: Optimal control law, Principle of optimality, principle of causality, principle of invariant imbedding, a recurrence relation of dynamic programming – computational procedure, Hamilton-Jacobi equation, and its application, one dimensional regulator problem and its solution using dynamic programming computational procedure. | 06 |
| ***Unit 3:*** | **Optimization Problems & Techniques**: Pontryagin's minimum principle, control & state variable inequality constraints, A nonlinear Reactor model problem and its solution, Minimum time problems, Minimization of functions, minimization of Functionals, two point boundary value problems. | 08 |
| ***Unit 4:*** | **Introduction:-**Adaptive Control (Identifier based & Non Identifier based), Applications, Linear feedback, effects of process disturbances, robustness, adaptive schemes and various adaptive control strategies, Parametric models, Parameter identification(One Parameter Case & two Parameter Case). | 07 |
| ***Unit 5:*** | **Model – Reference Adaptive System (MRAS) & Gain Scheduling:-** MRAS: MIT Rule, Lyapunov Theory, Design of MRAS using Lyapunov Theory, Relation between MRAS and STR, Non-Linear System: Feedback Linearization, Adaptive Feedback Linearization, Back-stepping, Adaptive | 07 |

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|---|---|---|
| | Back-stepping with tuning functions, Design of Gain- Scheduling Controllers | |
| **Total Hours** | | **36** |

| | *Textbooks and Reference Books* |
|---|---|
| **1.** | Donald E. Kirk, "***Optimal Control Theory: An Introduction"***, Prentice-Hall networks series, 10th Edition, 1970. |
| **2.** | Anderson .B. D. O, Moore .J. B, "***Optimal control linear Quadratic methods"***, Prentice Hall of India, 1th Edition, New Delhi, 1991. |
| | |
| **3.** | Sage A. P, White .C. C, "***Optimum Systems Control"***, 2nd Edition, Prentice Hall, 1977. |
| **4.** | Athans M and P L Falb, "***Optimal Control-An Introduction to the Theory and its Applications"***, McGraw Hill Inc, New York, 1th Edition,1966. |
| **5.** | Sage A P, "***Optimum Systems Control"***, Prentice –Hall Inc Englewood Cliffs, New Jersey, 2nd Edition, 1968 |

| **Mode of Evaluation** | Test / Quiz / Assignment / Mid Term Exam / End Term Exam. |
|---|---|